IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Case No. 01-181-A)

In re Application of:	)	
	)	
Huy Nguyen,et al.	)	Group Art Unit: 2819
	)	
Serial No.: 10/629,167	)	Examiner: Daniel D. Chang
	)	
Filed: July 28, 2003	)	
	)	
For: Apparatus and Method for Level-Shifting Input Receiver Circuit from High External Voltage to Low Internal Supply Voltage	)	

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Pursuant to the duty of disclosure provided by 35 C.F.R. § 1.56 and §§ 1.97-98, the applicants wish to make the following references and information of record in the above-identified application. The references are also listed in the PTO-1449 form enclosed herewith. It is requested that the references and information be given careful consideration and that they be cited of record in the prosecution history of the present application so that they will appear on the face of the patent issuing from the present application.

Pursuant to 37 C.F.R. § 1.98(d), copies of the references are not enclosed. These references were made of record in the parent application serial no. 09/849,755 filed May 4, 2001. A check in the amount of $310, which includes the $180 Information Disclosure

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Statement fee under 37 C.F.R. § 1.97(c)(2) and § 1.17(p) is enclosed herewith. Please charge any deficiency or credit any overpayment to Account No. 13-2490.

In the judgment of the undersigned, portions of the references may be material to the examination of the pending claims. No representation is intended as to the relative importance of any portion of the references. This Statement is not a representation that the cited references have effective dates early enough to be "prior art" within the meaning of 35 U.S.C. §§ 102 or 103.

CITED REFERENCESS

U. S. PATENTS

PATENT NO.	DATE ISSUED	INVENTOR	CLASSIFICATION	
5,534,795	07/09/96	Wert et al.	326	81
5,534,798	07/09/96	Phillips et al.	326	108
5,663,663	09/02/97	Cao et al.	326	81
5,751,168	05/12/98	Speed, III et al.	326	83
5,757,712	05/26/98	Nagel et al.	365	226
5,867,010	02/02/99	Hinedi et al.	323	282
5,973,508	10/26/99	Nowak et al.	326	81
5,986,472	11/16/99	Hinedi et al.	326	68
6,097,215	08/01/00	Bialas, Jr. et al.	326	68
6,160,421	12/12/00	Barna	326	63

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Other Documents

1. *"Direct Rambus Clock Generator"*, Rambus Inc., Document DL-0056, Version 1.2, November 2000, pages 1-22.
2. "Application Brief #1", IDT Logic Applications, Integrated Device Technology, Inc., APP-BRF1-00050, 2000, pages 1-4.
3. Jim Hagerman, *"Two Transistors Form Bidirectional Level Translator"*, www.ednmag.com/reg/1996/110796/23DI_02.htm, 1996, pages 1-3.
4. *"The PC Technology Guide"*, www.pctechguide.com/03memory.htm, February 18, 2001, pages 1-9.
5. *"System Management Bus (SMBus) Specification Version 2.0"*, Section 2 General Characteristics, SBS Implementers Forum, August 3, 2000, pages 9-10.
6. Kenneth M. Cuy, *"Design Considerations Bring Unity To A Mexed-Voltage World"*, www.ednmag.com/ednmag/reg/1995/020295/03df3.htm, February 2, 1995, pages 1-8.

Respectfully submitted,

McDonnell Boehnen Hulbert & Berghoff

Date: April 5, 2004 By: _____

Paul W. Churilla
Reg. No. 47,495

CERTIFICATE OF MAILING

The undersigned hereby certifies that the foregoing INFORMATION DISCLOSURE STATEMENT is being deposited as first class mail, postage prepaid, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 5 day of April, 2004.

_____

Paul W. Churilla

FORM PTO-1449 (Rev. 2-32)	U.S. Department of Commerce Patent and Trademark Office	Atty. Docket No.	Serial No.
	**INFORMATION DISCLOSURE STATEMENT BY APPLICANT** (Use several sheets if necessary)	01-181-A	10/629,167
		Applicant: Huy Nguyen, et al.	
		Filing Date: 07/28/03	**Group:** 2819

U.S. PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate
		5,534,795	07/09/96	Wert et al.	326	81	12/09/94
		5,534,798	07/09/96	Phillips et al.	326	108	06/06/95
		5,663,663	09/02/97	Cao et al.	326	81	04/26/96
		5,751,168	05/12/98	Speed, III et al.	326	83	04/28/95
		5,757,712	05/26/98	Nagel et al.	365	226	07/12/96
		5,867,010	02/02/99	Hinedi et al.	323	282	06/06/97
		5,973,508	10/26/99	Nowak et al.	326	81	05/21/97
		5,986,472	11/16/99	Hinedi et al.	326	68	06/06/97
		6,097,215	08/01/00	Bialas, Jr. et al.	326	68	05/22/98
		6,160,421	12/12/00	Barna	326	63	10/22/98

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication.

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		Filing Date: 07/28/03	Group: 2819

FOREIGN PATENT DOCUMENTS

		Document Number	Date	Country	Class	Subclass	Translation	
							Yes	No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc).

			"Direct Rambus Clock Generator", Rambus Inc., Document DL-0056, Version 1.2, November 2000, pages 1-22.
			"Application Brief #1", IDT Logic Applications, Integrated Device Technology, Inc., APP-BRF1-00050, 2000, pages 1-4.
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			"The PC Technology Guide", www.pctechguide.com/03memory.htm, February 18, 2001, pages 1-9.
			"System Management Bus (SMBus) Specification Version 2.0", Section 2 General Characteristics, SBS Implementers Forum, August 3, 2000, pages 9-10.
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